Docket No.: J0658.0018

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:
Jens Barrenscheen et al.

Application No.: 10/727,102 | Confirmation No.: 4397

Filed: December 2, 2003 | Art Unit: 2181

For: Arrangement comprising a first semiconductor chip and a second semiconductor chip connected thereto | Examiner: C. K. Lee

RESPONSE TO EXAMINER'S ANSWER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir or Madam:

Appellants submit this Reply Brief pursuant to 37 CFR § 41.41(a), and in response to the Examiner's Answer mailed on July 16, 2009, for the above identified U.S. Patent application. As required under § 41.41(a), this Reply Brief is filed within two months of the Examiner's Answer.

No fees are believed due for the filing of this Reply Brief. However, if any fee is due, the Patent Office is authorized to charge such fee to Deposit Account No. 50-2215.

As described in Appellants' Appeal Brief, claims 2-4, 6-20 and 22-25 stand improperly rejected under 35 U.S.C. § 103(a). Appellants maintain each argument presented in the Appeal Brief and submit this Reply Brief to address the Examiner's Response to Arguments as set forth on pages 22-24 of the Examiner's Answer.

In the "Response to Argument" section on pages 22-24 of the Examiner's Answer, and throughout the Rejection section, the Examiner's Answer has cited paragraphs [0006]-[0009] and [0046] of Balasundram. Specifically, the Examiner's Answer asserts that Balasundram in combination with Applicants' Admitted Prior Art discloses "a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip," as required by each of independent claims 23-25. Appellants respectfully reassert that this limitation is neither disclosed nor suggested by the prior art.

The Examiner's Answer appears to be equating Balasundram's use of time division multiplexing as a suggestion that Balasundram transmits a data frame with first and second portions intended for first and second semiconductor chips, respectively. This conclusion is improper. One skilled in the art knows that time division multiplexing is a process by which two or more channels of information are transmitted over the same link by allocating a different time interval for the transmission of each channel. In fact, the cited portion of Balasundram discloses that time division multiplexing involves systems in which each transmitter-receiver pair is typically allotted a particular time interval or channel to transmit signals over the communication line. (See paragraph [0008] of Balasundram.)

As such, one skilled in the art would know both generally and in light of Balasundram's teachings that Balasundram's system transmits data to the various receivers of its system at separate time intervals, not concurrently via the same frame. Balasundram therefore does not teach or suggest a portion of data on a frame is intended for a first, second semiconductor chip, and a portion of data on the same frame is intended for a second, second semiconductor chip, as required by the independent claims.

To further justify the rejection, the Examiner's Answer at page 22 asserts that Balasundram teaches time division multiplexing employing a single frame allocated to include two identifier addresses. This conclusion on its face must fail. Firstly, nowhere in Balasundram is this feature disclosed. And secondly, nowhere in Balasundram is this feature suggested since, as

discussed above, time division multiplexing involves sending data at separate time intervals. There is no way to reconcile transmitting data at separate time intervals with the explicitly recited limitation of transmitting two portions of data to two separate semiconductor chips via the same frame.

As previously noted in Appellants' Appeal Brief, because each of Balasundram's multiple byte waveform messages has a fixed leading byte, Balasundram inherently does not disclose that a plurality of data is transferred utilizing a single allotted time interval (e.g., a single frame). Accordingly, in light of the foregoing arguments, Appellants reassert that Balasundram neither alone nor in combination with Applicants' Admitted Prior Art discloses "a first portion of data transmitted in a frame is intended for a first, second semiconductor chip, and a second portion of the data transmitted in this frame is intended for a second, second semiconductor chip," as required by each of independent claims 23-25.

Accordingly, for at least the reasons set forth above, and those identified in the Appeal Brief, Appellants respectfully reassert that that the Examiner has maintained his rejection of the pending claims in error.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Appellants respectfully request that the Board order the withdrawal of the pending rejections so that the pending claims can pass to issue.

Dated: August 19, 2009

Respectfully submitted,

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